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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,439	11/16/2001	Nicholas E. Aneshansley	2070.005800/P6758	6089

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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,439	ANESHANSLEY, NICHOLAS E.	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 November 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/16/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by DROGICHEN (U.S. Patent 6,571,360).

As to claim 1, DROGICHEN teaches a method comprising: processing tasks associated with at least one processor (col. 5, lines 57-58), wherein the processor comprises at least one cache memory (contents of memory) having data stored therein (col. 5, lines 57-58); transferring at least a portion of the data of the cache memory to another location (via migrating the contents of memory to other boards) (col. 5, lines 57-58); and removing the processor from a system in response to transferring at least the portion of the data from the cache memory to another location, while the system is in operation (The dynamic reconfiguration can be performed while the computer ystem is in operation and the processors are taken offline and later physically removed from the system) (col. 5, line 47 – col. 6, line 5).

As to claim 2, DROGICHEN teaches transferring at least the portion of the data of the cache memory to another location comprises transferring at least the portion of the data of the cache memory to non-cache memory in the system (col. 5, line 57 – col. 6, line 5).

As to claim 3, DROGICHEN teaches a domain defined therein, wherein transferring at least the portion of the data comprises transferring at least the portion of the data of the cache memory of the domain to non-cache memory of the domain in the system (col. 5, line 57 – col. 6, line 5).

As to claim 4, DROGICHEN teaches removing the processor from the system comprises removing a board comprising the processor and the cache memory from the system (physically remove the board) (col. 6, lines 1-5).

As to claim 5, DROGICHEN teaches removing the board comprises removing the board from the domain in the system (col. 5, line 57 – col. 6, line 5).

As to claim 11, DROGICHEN teaches an apparatus, comprising: at least one processor (processor / board) to execute one or more assigned tasks (process execution) (col. 5, lines 57-58); and an interface to couple the apparatus to a system, wherein the apparatus is adapted to be removed from the system in response to executing the one or more assigned tasks, while the system is in operation (via the

system administrator using the system controller to dynamic configure various microprocessor and I/O boards into the system dynamically) (col. 5, lines 40 – col. 6, line 5).

As to claim 16, DROGICHEN teaches a system comprising: an interface adapted to receive a first processor (processor / I/O board) and an associated cache memory; a control unit adapted to cause at least a portion of the contents of the associated cache memory to be transferred to a second memory location (migrate contents of memory to other boards) and, in response to the transfer, the first processor to be removed from a domain of the system, while the system is in operation (via the system administrator using the system controller to dynamic configure various microprocessor and I/O boards into the system dynamically by removing and attaching processors and I/O boards) (col. 5, lines 40 – col. 6, line 5).

As to claim 23, DROGICHEN teaches a system comprising: a first board having a memory element (microprocessor and I/O boards); a second board having a processor an only a cache memory element (other boards), wherein the processor is adapted to execute one or more current tasks (process execution); a control unit adapted to receive an indication to dynamically remove the second board from a domain of the system, wherein the control unit, in response to receiving the indication, is adapted to process at least one current tasks associated with the processor and transfer at least a portion of data stored in the cache memory on the second board to

the memory element of the first board (via the system administrator using the system controller to dynamic configure various microprocessor and I/O boards into the system dynamically by removing and attaching processors and I/O boards) (col. 5, lines 40 – col. 6, line 5)..

As to claim 26, DROGICHEN teaches an apparatus, comprising: at least two processors (microprocessor board / control boards / I/O board), wherein each processor has at least one associated cache memory but no non-cache memory (col. 5, lines 57-58); an address repeater coupled to the two processors, wherein the address repeater is adapted to receive at least one data request and to provide the request to at least one of the two processors (via the system interconnect bus) (col. 4, lines 5-20); a data crossbar (centerplane) (col. 3, lines 64-66); a dual CPU data switch (control and arbitration subsystems) coupled to the two processor and the crossbar, wherein the dual CPU data switch is adapted to provide data from at least one of the cache memories of the two processor to the data crossbar in response to the received data request; (via the centerplane containing two symmetrical sides that can each mount multiple expander boards and a system control board wherein communication is communicated through the interconnect bus and supported by control and arbitration subsystems) (col. 4, lines 1-20); and a data controller coupled to the network wherein the data controller is adapted to indicate to the network where to send the requested data (via the system administrator using the system controller to dynamic configure

various microprocessor and I/O boards into the system dynamically by removing and attaching processors and I/O boards) (col. 5, lines 40 – col. 6, line 5).

As to claims 28-32, reference is made to an article that corresponds to the method of claims 1-5 and is therefore met by the rejection of claims 1-5 above.

As to claim 6, DROGICHEN teaches processing the tasks associated with the at least one processor comprises stopping new tasks from being assigned to the processor (via taking the processor offline) (col. 5, lines 47-col. 6, line 5).

As to claim 7, DROGHICHEN teaches processing the tasks comprises allowing the processor to substantially complete current tasks (via performing all other operating system task before taking the processor offline) (col. 5, lines 47 – col. 6, line 5).

As to claim 8, DROGHICHEN teaches processing the tasks comprises flushing the current state of the processor (via the operating system flushes all pageable memory to disk) (col. 5, line 47 – col. 6, line 5).

As to claim 9, DROGHICHEN teaches processing the tasks comprises sending an acknowledgement signal indicating that is safe to remove the board (via placing the processor in an offline state such that the centerplane hardware isolates the component

from is previous system to available to be physically removed) (col. 5, line 47 – col. 6, line 5).

As to claim 10, DROGHICHEN teaches transferring at least a portion of the data comprises transferring all of the data stored in the cache memory (via migrating the contents of memory) (col. 5, line 47 – col. 6, line 5).

As to claim 12, DROGHICHEN teaches the processor comprises at least one associated cache memory element having data stored therein (via migrating the contents of memory) (col. 5, line 47 – col. 5, line 5).

As to claim 13, DROGHICHEN teaches the device is adapted to be removed from the system in response to transferring a portion of the data of the cache memory to a non-cache memory external to the apparatus (via migrating the contents of memory) (col. 5, line 47 – col. 6, line 5).

As to claim 14, DROGHICHEN teaches the portion of the data comprises all the data stored in the cache memory (col. 5, line 47- col. 6, line 5).

As to claim 15, DROGHICHEN teaches the processor is adapted to transmit a signal to the system when the processor has substantially completed the one or more assigned task via placing the processor in an offline state such that the centerplane

hardware isolates the component from is previous system to available to be physically removed) (col. 5, line 47 – col. 6, line 5).

As to claim 17, DROGHICHEN teaches the domain comprises at least one additional processor that continues to operate for at least a selected duration after the removal of the first processor (other boards wherein information is migrated to) (col. 5, line 47 – col. 6, line 5).

As to claim 18, DROGHICHEN teaches the second memory location comprises a non-cache memory in the domain (memory) (col. 5, line 47 – col. 6, line 5).

As to claim 19, DROGHICHEN teaches the second processor is further adapted to stop the assignment of additional tasks to the first processor (via taking the processor offline) (col. 5, lines 47-col. 6, line 5).

As to claim 20, DROGHICHEN teaches the second processor is further adapted to allow the first processor to substantially complete the current tasks (via performing all other operating system task before taking the processor offline) (col. 5, lines 47 – col. 6, line 5).

As to claim 21, DROGHICHEN teaches the second processor is adapted to reassign current tasks (via migrating process execution) (col. 5, line 47 – col. 6, line 5).

As to claim 22, DROGHICHEN teaches the second processor is adapted to flush the current state of the first processor (via the operating system flushes all pageable memory to disk) (col. 5, line 47 – col. 6, line 5).

As to claim 24, DROGHICHEN teaches the control unit is adapted to allow the processor on the second board to complete the one or more current tasks (via performing all other operating system task before taking the processor offline) (col. 5, lines 47 – col. 6, line 5).

As to claim 25, DROGHICHEN teaches the first board comprises a processor and wherein the control unit is adapted to reassign at least one of the current tasks associated with the processor of the second board to the processor of the first board (via migrating process execution) (col. 5, line 47 – col. 6, line 5).

As to claim 27, DROGHICHEN teaches at least one of the processors is adapted to send data address requests through the address repeater and receive the requested data through the data crossbar and dual CPU data switch (via the centerplane containing two symmetrical sides that can each mount multiple expander boards and a system control board wherein communication is communicated through the interconnect bus and supported by control and arbitration subsystems) (col. 4, lines 1-20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 30, 2005

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER